REMARKS/ARGUMENTS

Status of Claims

Claims 1-5 and 7-18 are pending in this application, with claim 1 being the only independent claim. Claim 15 has been cancelled without prejudice or disclaimer. Independent claim 1 has been amended to incorporate additional features disclosed in paragraph [0036] of applicants' published application (see US 2007/0034880). New claims 16-18 recite subject matter disclosed in paragraph [0030] of applicants' published application. No new matter has been added.

Reconsideration of the subject application in view of the claim amendments and the following remarks is hereby requested.

Overview of the Office Action

Claim 15 has been objected to for informalities.

Claims 1-7 and 9-15 have been rejected under 35 U.S.C. § 103(a) as unpatentable over US 6,100,104 ("Haerle") in view of US 5,659,184 ("Tokunaga").

Claims 9-11 have been rejected under 35 U.S.C. § 103(a) as unpatentable over Haerle in view of Tokunaga, and further in view of US 6,110,277 ("Braun").

Patentability of the Claimed Invention

A. Independent Claim 1

Independent claim 1 now recites that "the windows of the mask material layer comprise a plurality of statistically distributed windows having varying forms and opening areas." This added feature of amended independent claim 1 is not taught by the combination of Haerle and Tokunaga.

Haerle discloses a method for forming a plurality semiconductor chips in the openings (windows) 10 of a mask layer 4. According to Haerle, a mask layer 4 is formed on a substrate wafer 19 and then photopatterned to form a plurality of windows 10 in the mask layer 4 (see Figs. 1 and 3). A semiconductor sequence 18, including a light-emitting layer 23, is epitaxially deposited in the windows 10, followed by the application of front-side contact metallization layers 15 to each semiconductor body to make contact with the LED structure 2 (see Figs. 4 and 5; col. 6, ll. 59; and col. 7, ll. 13-24).

As depicted in Figs. 3 through 5 of Haerle, the windows 10 in Haerle's mask layer 4 have the same size and form, so as to define the size and form of the individual identical semiconductor chips to be fabricated. For example, each window 10 in Haerle has two mutually opposite plane-parallel side surfaces 7, which, in turn, define the two laser mirror surfaces 8 of the edge-emitting laser structure 2 (see, also, col. 3, ll. 45-50 of Haerle). Since the individual semiconductor chips to be fabricated in Haerle are of the same size and form, the windows 10 which define the size and form of such individual semiconductor chips thus are likewise of the same size and form as is apparent to one skilled in the art. Therefore, Haerle's windows 10 do not have "varying forms and opening areas" as expressly recited in amended independent claim 1. Haerle does not teach each and every claim feature recited in amended independent claim 1 for at least this reason.

There is also no teaching in Haerle that its windows 10 are "statistically distributed," as are the claimed multiplicity of windows recited in amended independent claim 1. Indeed, the windows 10 in Haerle are formed by photopatterning the mask layer 4. Consequently, as one skilled in the art will appreciate, the windows 10 in Haerle are not "statistically distributed," as expressly recited in amended independent claim 1. Haerle does not therefore teach each and every claim feature recited in amended independent claim 1 for this additional reason.

Moreover, in view of the above teachings of Haerle, there is a total lack of reason or motivation for one skilled in the art to modify Haerle's mask layer 4 in such a way as to form "statistically distributed windows having varying forms and opening areas," as now recited in independent claim 1. For one thing, such a modification of Haerle would result in multiple semiconductor chips that are statistically distributed on the wafer and have different sizes, forms and operating characteristic and/or functions, and thus depart from the teachings and instructions of Haerle. The above-recited claim features of amended claim 1 are therefore not rendered obvious in view by the teachings of Haerle.

Tokunaga is cited in the Office Action for its alleged teachings of an optoelectronic semiconductor chip having a plurality of structural elements each containing a semiconductor layer sequence and of windows having an average extent of less than 2 micrometers (see page 4 of the Office Action). Without admitting or disputing this interpretation of Tokunaga, applicants point out that Tokunaga does not remedy the above-discussed deficiencies of Haerle.

Tokunaga discloses a method for forming a III-V compound semiconductor device. For example, Tokunaga teaches forming opening small windows in the mask layer by etching (see col. 7, ll 50-56 and in Figs. 1L and 1M of Tokunaga). A III-V compound is grown in areas of the windows in the film 102 (see Figs. 1D-1F). In Tokunaga, the nucleation surfaces are square-shaped with a side "a" and are arranged in a lattice pattern with a pitch "b" between the centers (see Fig. 6 and col. 6, ll. 58-61 of Tokunaga).

There is no teaching or suggestion in Tokunaga that these nucleation surfaces are either "statistically distributed" or of "varying forms or opening areas," as now expressly recited in independent claim 1. In contrast, the nucleation surfaces in Tokunaga are shown to be evenly distributed and of a uniform shape and form (see, e.g., Fig. 6 of Tokunage). Tokunaga does not therefore teach that "the windows of the mask material layer comprise a plurality of statistically

distributed windows having varying forms and opening areas", as now expressly recited in amended claim 1, or otherwise remedy the above-discussed deficiencies of Haerle.

In view of the foregoing, independent claim 1 as amended patentably distinguishes over the cited combination of Haerle and Tokunaga. The 35 U.S.C. § 103(a) rejection of independent claim 1 should accordingly be reconsidered and withdrawn.

B. Dependent Claims 2-5 and 7-18

Claims 2-5 and 7-18 depend, directly or indirectly, from allowable independent claim 1 and thus are each deemed to be allowable therewith. In addition, these dependent claims each include features that serve to still further distinguish the claimed invention over the cited prior art.

Conclusion

In view of the foregoing, reconsideration, withdrawal of all rejections and allowance of all pending claims are respectfully solicited. Should the Examiner have any comments, questions, suggestions, or objections, the Examiner is respectfully requested to telephone the undersigned to facilitate an early resolution of any outstanding issues.

No fees or charges are required with this Submission. However, if any such fees or charges are required at this time, they may be charged to our USPTO Deposit Account No. 03-2412.

Respectfully submitted,
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